REMARKS

In the Official Action, the Examiner rejected claims 1-4, 7-10, 12, 13, 15-18, 20-22, 25, 27, 30, 45, 47, 48, and 50. Applicants respectfully request reconsideration of the application in view of the remarks set forth below. Applicants believe that all pending claims are in condition for allowance.

Information Disclosure Statement

The Examiner stated that the information disclosure statement filed August 6, 2001 failed to comply with 37 C.F.R. 1.98(a)(2), which requires a legible copy of each cited non-patent literature publication or that portion of which cause it to be listed. Accordingly, Applicants hereby resubmit a legible copy of the non-patent literature publication "Nonvolatile Timekeeping RAM," (attached hereto as "Appendix A") for the Examiner to consider.

Claim Rejections under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-4, 7-10, 12, 13, 15-18, 20-22, 25, 27, 30, 45, 47, 48, and 50 under U.S.C. § 102(b) as being unpatentable over Selph et al. (U.S. Patent No. 4,804,957, hereafter "the Selph reference"). With regards to the independent claims, the Examiner stated:

> Regarding claim 1, Selph et al. disclose a method of detecting removal of a component of an electrical system, comprising triggering a detection circuit upon removal of a component (see column 6, lines 52-68), disconnecting a counter within the detection circuit to retain data related to when the intrusion occurred (see column 12, lines 45-56; column 16, lines 28-58), and storing the retained data in non-volatile memory (see column 9 lines 38-60; column 12, lines 45-56; column 16, lines 28-58).

> Regarding claim 15-17, Selph et al. disclose a method for detecting loss of power to a portion of a computer system, comprising triggering a detection circuit upon loss of power (see abstract column 16, lines 49-58), disconnecting a counter within the detection circuit to retain data related to when the loss of power occurred (see column 12, lines 45-56; column 16, liens 49-58), and storing the retained data in non-volatile memory (see abstract; column 3, lines 12-34; column 9, lines 38-41; column 12, lines 45-56; column 16, lines 28-5). Note that a microprocessor-based circuit that is used to measure, analyze, determine information, and stare in random access memory is a computer.
>
> Regarding claim 21, 22, and 25, Selph et al. disclose a method for detecting removal of a component of a system, comprising generating an alarm signal (see abstract; column 3, lines 35-51; column 6, lines 52-68), using the signal to stop a clock, and recording the value of the clock 9see column 12, liens 45-56; column 16, lines 28-58).
>
> Regarding claim 45, Selph et al disclose a computer system comprising:
>
> chassis with a removable cover providing internal access to the chassis, the chassis housing internal components of the computer (see column 6, lines 52-69).
>
> a microprocessor operatively connected to detect inputs from an input device, and memory which is connected to be read/write accessible by the microprocessor (see column 2, line 59 - column 3, line 11);
>
> one or more devices for mass storage of data, and an output device operatively connected to receive outputs from the microprocessor (see column 9, lines 38-60);
>
> one or more power supplies connected to provide power to the internal components (see column 9, lines 61-67); and
>
> a detection circuit which stores data releated to when the removable cover is removed (see column 6, liens 52-69; column 10, lines 17-36; column 11, lines 30-46; column 12, lines 45-56; column 16, lines 28-58).

Office Action, pp. 3-4.

Applicants respectfully traverse this rejection. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under

Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

The present application discloses an intrusion detection mechanism which stores the time and date that a chassis hood, system component or AC power is removed from a computer system. Abstract. For example, if the chassis hood is opened, a system component is removed or AC power is removed, a switch in the computer system opens and an alarm bit is set. Page 6, lines 22-23; *see also* page 8, lines 29-31; *see also* page 9, lines 14-15; *see also* page 11, lines 4-5. By opening the switch, a counter or clock is disconnected or stopped, thereby preserving the date and time of the intrusion event. Page 6, lines 25-26. The date and time information can be recorded/stored in non-volatile memory for use by a system administrator. Page 6, line 29 - page 7, line 7; abstract.

Accordingly, independent claim 1 recites a method of detecting removal of a component of an electrical system, comprising "triggering a detection circuit upon removal of a component," "disconnecting a counter within the detection circuit to retain data related to when said component was removed," and "storing the retained data in non-volatile memory." Similarly, independent claim 15 recites a method for detecting loss of power to a portion of a system, comprising "triggering a detection circuit upon loss of power," "disconnecting a counter within the detection circuit to retain data related to when said loss of power occurred," and "storing the retained data in non-volatile memory." Independent claim 21 recites a method for detecting

removal of a component of a system, comprising "when a component is removed generating a signal," "using said signal to stop a clock," and "recording the value of said clock." Independent claim 45 recites a computer system comprising "a detection circuit comprising an internal clock and which stores data related to when said components or said removable cover is removed."

In stark contrast, the Selph reference is directed to meters for measuring utilities consumed at a residence or business and more particularly to a microprocessor-based automatic remote metering system for measuring the consumption of utilities, such as electrical power, water, gas and the like. Col. 1, lines 12-17. In other words, the Selph reference is directed to a system for monitoring power usage (or the consumption of other utilities) at one or more locations. More specifically, the Selph reference discloses a system for providing time of use information relating to the instantaneous consumption of power at a preselected time such that correct billing rates may be applied. *See* Col. 2, lines 3-31.

Thus, the Selph reference is not directed to detecting and storing information regarding the removal or theft of computer components, as set forth in the present application. In contrast to the Examiner's assertions, the Selph reference only discloses recording time of use information related to *power consumption*. While the Selph reference does indeed disclose that a tamper detection device may be included in the system to transmit a tamper alert signal to a home office or monitoring substation (Col. 3, lines 39-44), the only discussion of such a device is simply directed at *detecting* the removal of the computer housing enclosure. Specifically, "a microswitch 67 or other sensor can be positioned to contact the enclosure 66 so that removal of the enclosure will be detected." Col. 6, lines 59-61. There is no further discussion regarding the microswitch 67 in the Selph reference. Accordingly, though the reference does summarily discuss *detecting* the removal of a computer housing enclosure, the Selph reference *does not* disclose

"disconnecting a counter within the detection circuit to retain data related to when said component was removed," nor does it disclose "storing the retained data in non-volatile memory," as recited in claim 1. Similarly, the Selph reference does not disclose "disconnecting a counter within the detection circuit to retain data related to when said loss of power occurred," nor does it disclose "storing the retained data in non-volatile memory," as recited in claim 15. Further, the Selph reference does not disclose generating a signal when a component is removed from a computer system, "using said signal to stop a clock," and "recording the value of said clock," as recited in claim 21. Finally, the Selph reference does not disclose "a detection circuit comprising an internal clock and which stores data related to when said components or said removable cover is removed."

In summary and as discussed in detail below, the Selph reference does not disclose *disconnecting a counter* when a component is removed or AC power is lost, nor does it disclose *storing the timing information* related to such an event, as recited in the present claims. At most, the Selph reference simply discloses a device (microswitch 67) which is capable of detecting the removal of a system housing.

In the Office Action, the Examiner cited the digital clock circuit 394 as correlating to the recited counter/clock. However, it is clear from the Selph reference that the digital clock circuit 394 is simply provided to aid in recording time of use information related to power consumption. "In order to provide the capability of recording time of use information, and in order to determine when peak utility demand has occurred, the data collection computer includes a digital clock circuit 394." Col. 16, lines 28-33. There is no correlation of the digital clock circuit 394 with the removal of computer components or power from the system. As such, the digital clock circuit 394 of the Selph reference is not disconnected or stopped upon the removal of system

components or power, as recited in the present claims. For this reason alone, the Selph reference cannot possibly anticipate the subject matter recited in independent claims 1, 15, 21, 45 or the claims dependent thereon.

Further, the Selph reference does not disclose storing or recording timing information related to the removal of a system component or power from the system as further recited in the present claims. The Examiner cited the non-volatile data storage memory 156 as correlating to the presently recited non-volatile memory. However, Applicants respectfully assert that there is nothing in the Selph reference to suggest that data, corresponding to the time that a system component or power is removed from the system, is stored in the data storage memory 156. Accordingly, Applicants respectfully assert that the Selph reference does not disclose this additionally recited feature of the present claims. Because the Selph reference fails to disclose each of the features recited in the present claims, the reference cannot possibly anticipate the recited subject matter. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of independent claims 1, 15, 21 and 45, as well as those claims dependent thereon.

Claim Rejections under 35 U.S.C. § 103(a)

The Examiner rejected claims 4, 7, 18, 20, 47, and 48 under 35 U.S.C. § 103(a) as obvious over the Selph reference in view of Cummings et al. (U.S. Patent No. 5,406,260, hereafter "the Cummings reference").

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed

invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d. 1430 (Fed. Cir. 1990). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

As discussed above with regard to the rejections under 35 U.S.C. § 102, the Selph reference does not disclose all of the elements recited in independent claims 1, 15, 21, and 45. The present rejection under 35 U.S.C. § 103 cites Selph as a primary reference for the rejection of dependent claims 4, 7, 18, 20, 47 and 48. Applicants respectfully submit that Cummings reference does nothing to cure the deficiencies of the Selph reference as discussed above with respect to the independent claims. Accordingly, Applicants respectfully submit that Selph alone nor in combination with Cummings discloses or suggests all of the elements recited in the present claims, and thus cannot possibly render the recited subject matter obvious. Thus, Applicants respectfully request withdrawal of the Examiner's rejections under 35 U.S.C. § 103(a) and allowance of claims 4, 7, 18, 20, 47 and 48.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of all pending claims 1-4, 7-10, 12, 13, 15-18, 20-22, 25, 27, 30, 45, 47, 48, and 50. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: September 21, 2005

Robert A. Manware
Reg. No. 48,758
(281) 970-4545

Correspondence Address:

Hewlett-Packard Company
IP Administration
Legal Department, M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400

Appendix A

DALLAS SEMICONDUCTOR MAXIM

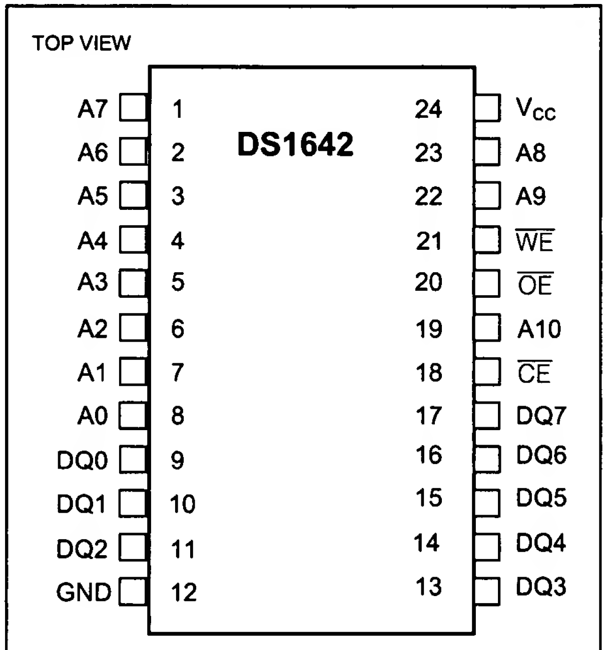
DS1642
Nonvolatile Timekeeping RAM

www.maxim-ic.com

FEATURES

- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Standard JEDEC Bytewide 2k x 8 Static RAM Pinout
- Clock Registers are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- Access Times of 70ns and 100ns
- Quartz Accuracy ±1 Minute a Month at +25°C, Factory Calibrated
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Leap Year Compensation Valid Up to 2100
- Power-Fail Write Protection Allows for ±10% V_{CC} Power Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- UL Recognized

PIN CONFIGURATION



ENCAPSULATED DIP

ORDERING INFORMATION

PART	VOLTAGE RANGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1642-70+	5.0	0°C to +70°C	24 EDIP (0.720a)	DS1642-70+
DS1642-70	5.0	0°C to +70°C	24 EDIP (0.720a)	DS1642-70
DS1642-100+	5.0	0°C to +70°C	24 EDIP (0.720a)	DS1642-100+
DS1642-100	5.0	0°C to +70°C	24 EDIP (0.720a)	DS1642-100

**DS9034-PCX, DS9034I-PCX, DS9034-PCX+ required (must be ordered separately).*

A "+" indicates a lead-free product. The top mark will include a "+" symbol on lead-free devices.

REV: 041305

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	A7	Address Input
2	A6	
3	A5	
4	A4	
5	A3	
6	A2	
7	A1	
8	A0	
19	A10	
22	A9	
23	A8	
9	DQ0	Data Input/Output
10	DQ1	
11	DQ2	
13	DQ3	
14	DQ4	
15	DQ5	
16	DQ6	
17	DQ7	
12	GND	Ground
18	$\overline{CE}$	Active-Low Chip-Enable Input
20	$\overline{OE}$	Active-Low Output-Enable Input
21	$\overline{WE}$	Active-Low Write-Enable Input
24	V_{CC}	Power-Supply Input

DESCRIPTION

The DS1642 is a 2k x 8 nonvolatile static RAM and a full-function real-time clock (RTC), both of which are accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC-standard 2k x 8 SRAM. The device can also be easily substituted in ROM, EPROM, and EEPROM sockets, providing read/write nonvolatility and the addition of the real-time clock function. The real-time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1642 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS–READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1642 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1642 registers are updated simultaneously after the clock status is reset. Updating occurs within a second after the read bit is written to 0.

Figure 1. DS1642 BLOCK DIAGRAM

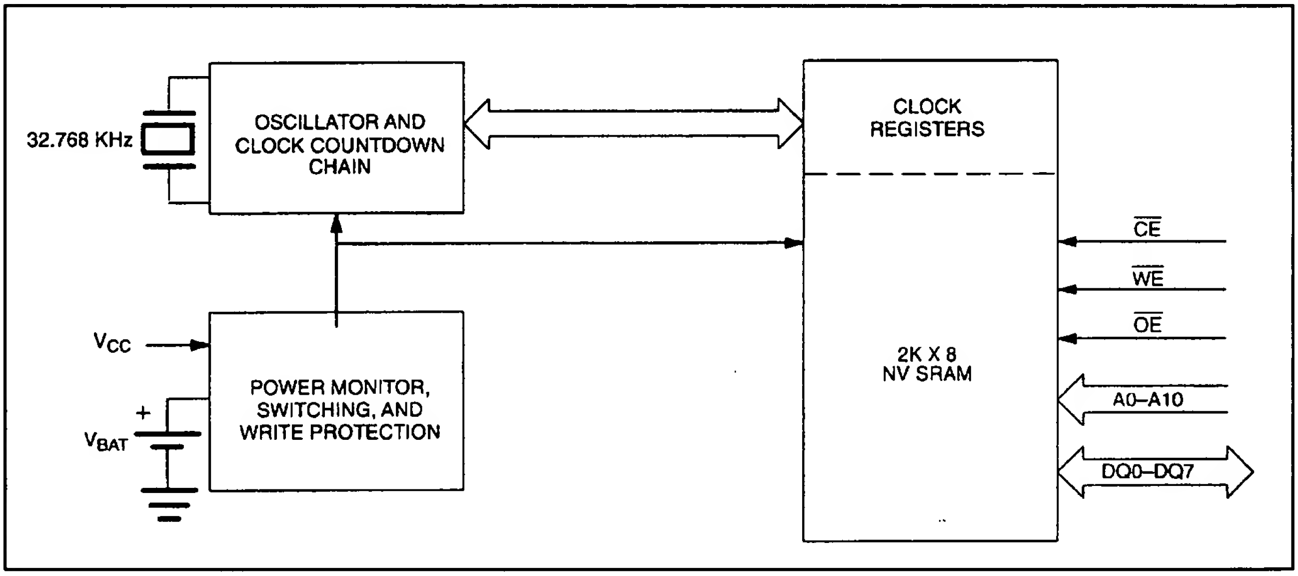


Table 1. TRUTH TABLE

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5V ±10%	V_{IH}	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
<4.5V > V_{BAT}	X	X	X	Deselect	High-Z	CMOS Standby
<V_{BAT}	X	X	X	Deselect	High-Z	Data Retention Mode

SETTING THE CLOCK

The 8th bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1642 registers. The user can then load them with the correct day, date and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{\text{OSC}}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{\text{CE}}$ low, and $\overline{\text{OE}}$ low) and address for seconds register remain valid and stable.

CLOCK ACCURACY

The DS1642 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. Dallas Semiconductor calibrates the clock at the factory by using special calibration nonvolatile-tuning elements. The DS1642 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary.

Table 2. REGISTER MAP–BANK1

ADDRESS	DATA								FUNCTION	
	B7	B6	B5	B4	B3	B2	B1	B0		
7FF	—	—	—	—	—	—	—	—	Year	00–99
7FE	X	X	X	—	—	—	—	—	Month	01–12
7FD	X	X	—	—	—	—	—	—	Date	01–31
7FC	X	FT	X	X	X	—	—	—	Day	00–23
7FB	X	X	—	—	—	—	—	—	Hour	00–59
7FA	X	—	—	—	—	—	—	—	Minutes	00–59
7F9	$\overline{\text{OSC}}$	—	—	—	—	—	—	—	Seconds	00–59
7F8	W	R	X	X	X	X	X	X	Control	A

$\overline{\text{OSC}}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

Note: All indicated "X" bits are not used but must be set to "0" during write cycle to ensure proper clock operation.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1642 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1642 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits ($V_{CC} > 4.5V$) the DS1642 can be accessed as described above by read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

BATTERY LONGEVITY

The DS1642 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1642 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1642 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1642 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground..-0.3V to +7.0V
Operating Temperature Range..0°C to +70°C (noncondensing)
Storage Temperature Range...-20°C to +70°C
Soldering Temperature...................................See IPC/JEDEC J-STD-020 (DIP Package) (Note 7)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage (All Inputs)	V_{IH}	2.2		V_{CC} + 0.3	V	1
Logic 0 Voltage (All Inputs)	V_{IL}	-0.3		0.8	V	1

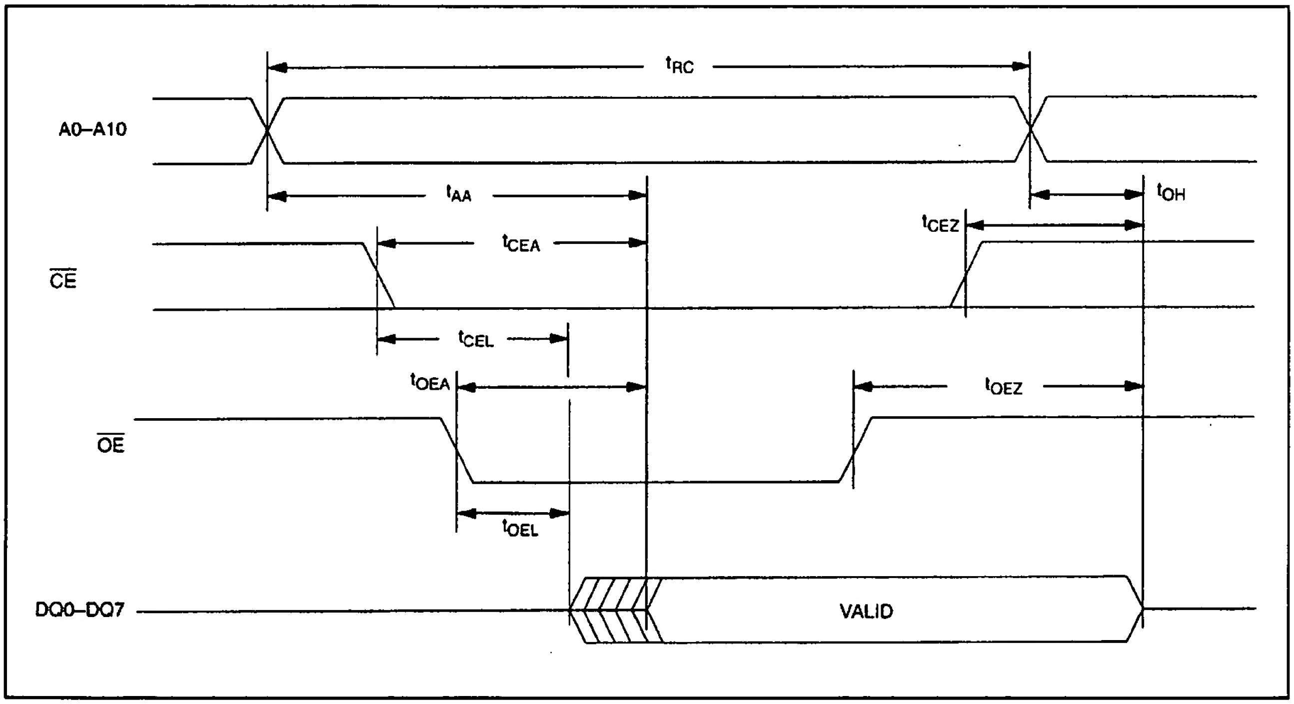
DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE}$ $\leq V_{CC}$ - 0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
I/O Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25	4.37	4.50	V	1

AC CHARACTERISTICS—READ CYCLE

PARAMETER	SYMBOL	70ns ACCESS		100ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Address Access Time	t_{AA}		70		100	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
$\overline{CE}$ Access Time	t_{CEA}		70		100	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		25		35	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		35		55	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}		25		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	

READ CYCLE TIMING DIAGRAM

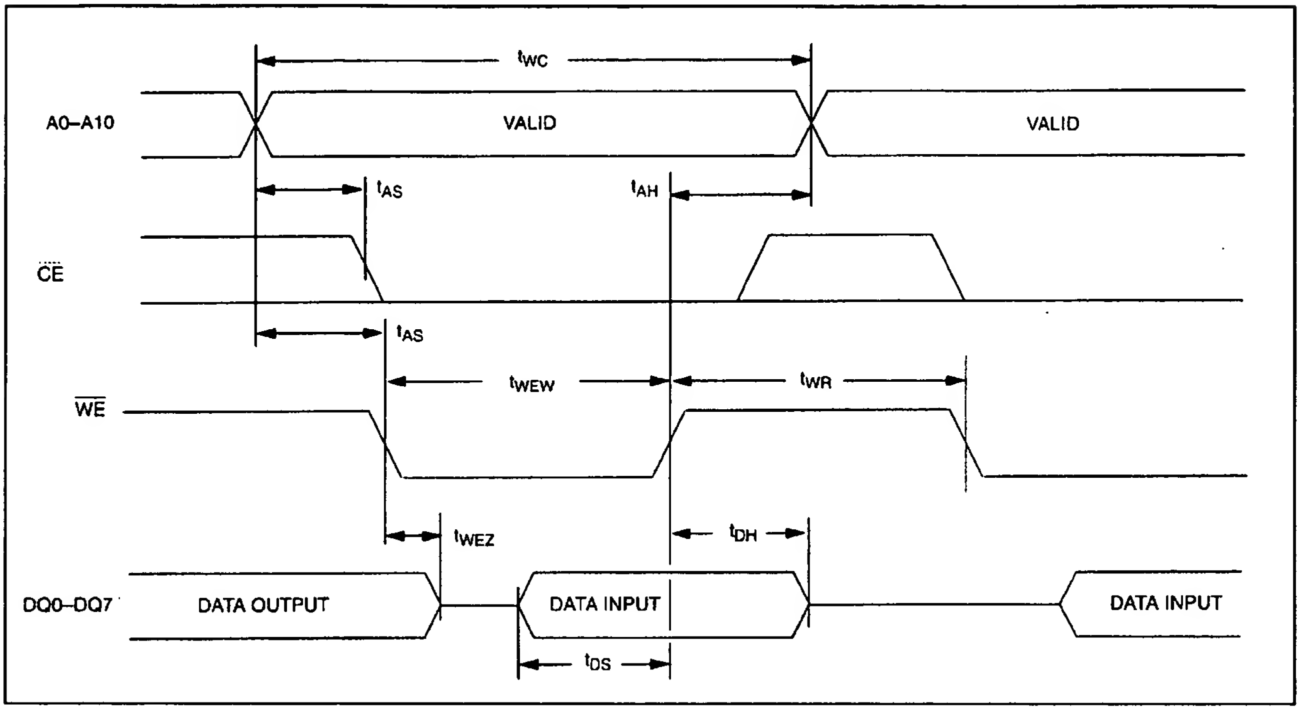


AC CHARACTERISTICS—WRITE CYCLE

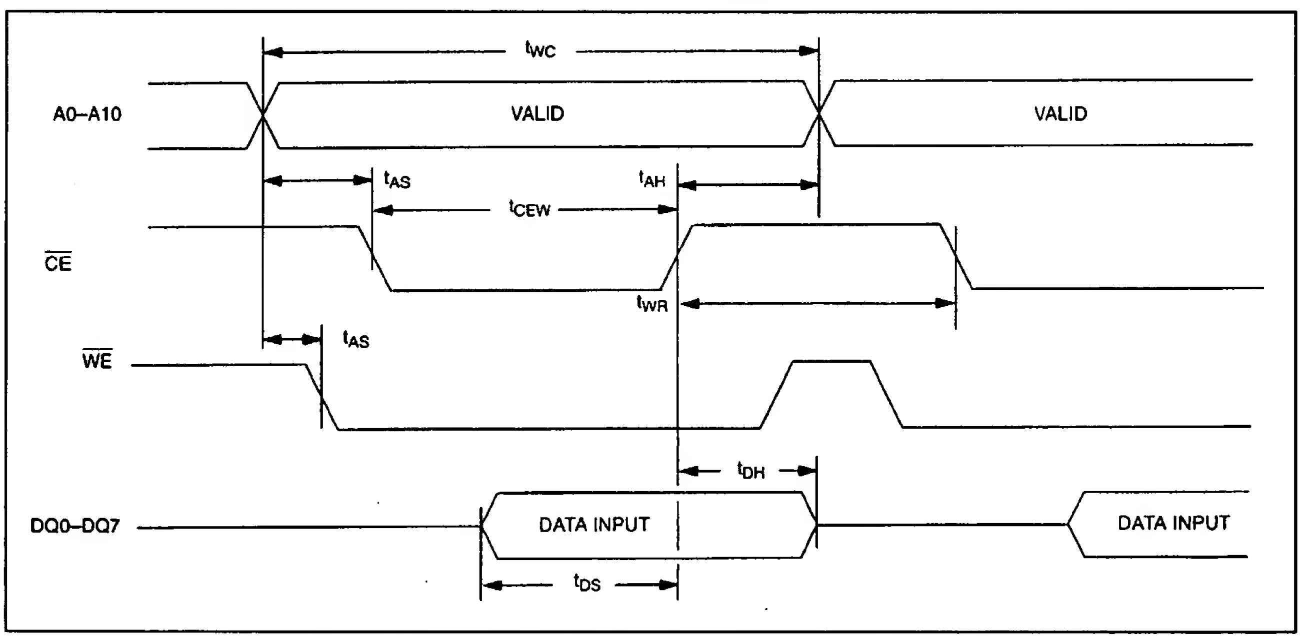
(V_{CC} = 5.0V ±10, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	70ns ACCESS		100ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	70		100		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{\text{WE}}$ Pulse Width	t_{WEW}	50		70		ns	
$\overline{\text{CE}}$ Pulse Width	t_{CEW}	60		75		ns	
Data Setup Time	t_{DS}	30		40		ns	
Data Hold Time	t_{DH}	0		0		ns	
Address Hold Time	t_{AH}	5		5		ns	
$\overline{\text{WE}}$ Data Off Time	t_{WEZ}		25		35	ns	
Write Recovery Time	t_{WR}	5		5		ns	

WRITE CYCLE TIMING DIAGRAM—WRITE-ENABLE CONTROLLED



WRITE CYCLE TIMING DIAGRAM—CHIP-ENABLE CONTROLLED

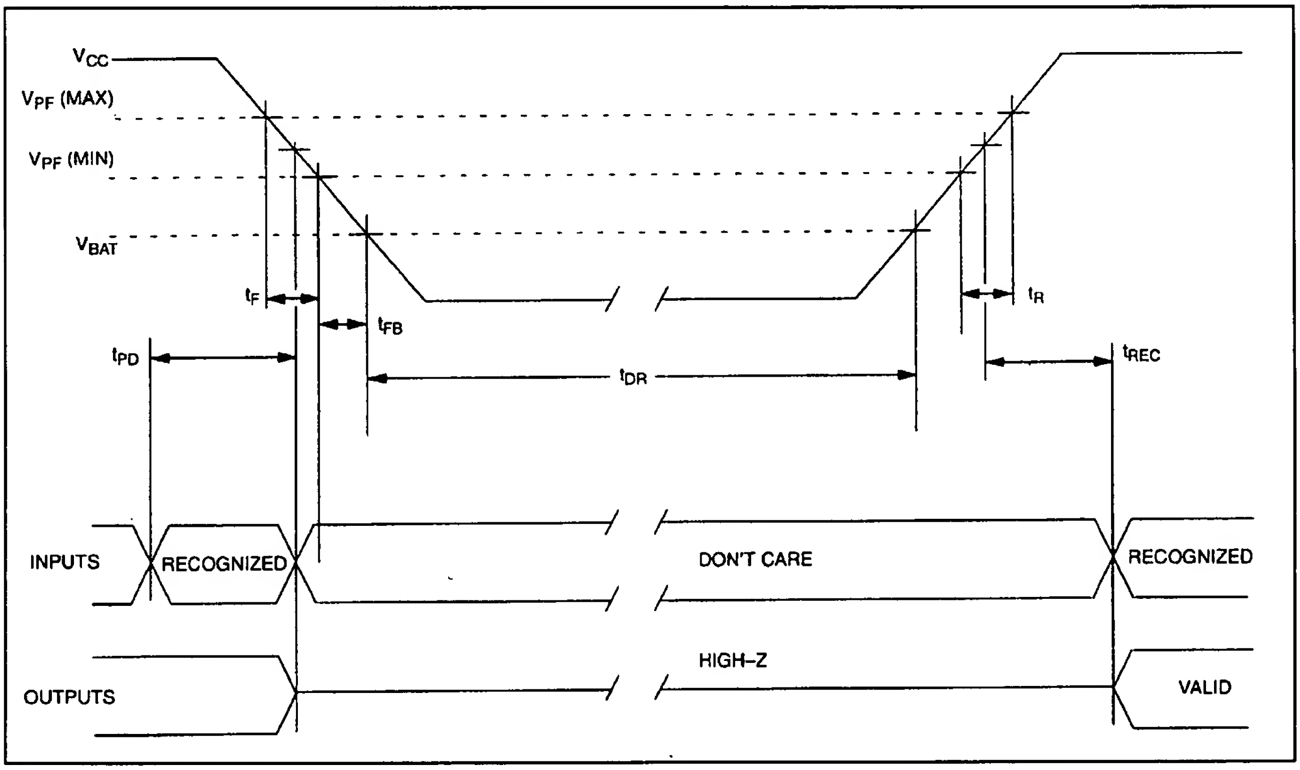


POWER-UP/POWER-DOWN AC CHARACTERISTICS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: V_{PF} (MAX) to V_{PF} (MIN)	t_F	300			µs	
V_{CC} Fall Time: V_{PF} (MIN) to V_{BAT}	t_{FB}	10			µs	
V_{CC} Rise Time: V_{PF} (MIN) to V_{PF} (MAX)	t_R	0			µs	
Power-up Recover Time	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4, 5

POWER-UP/POWER-DOWN WAVEFORM TIMING



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Pins (except DQ)	C_{IN}			7	pF	
Capacitance on DQ Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0.0 to 3.0V
Timing Measurement Reference Levels:
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

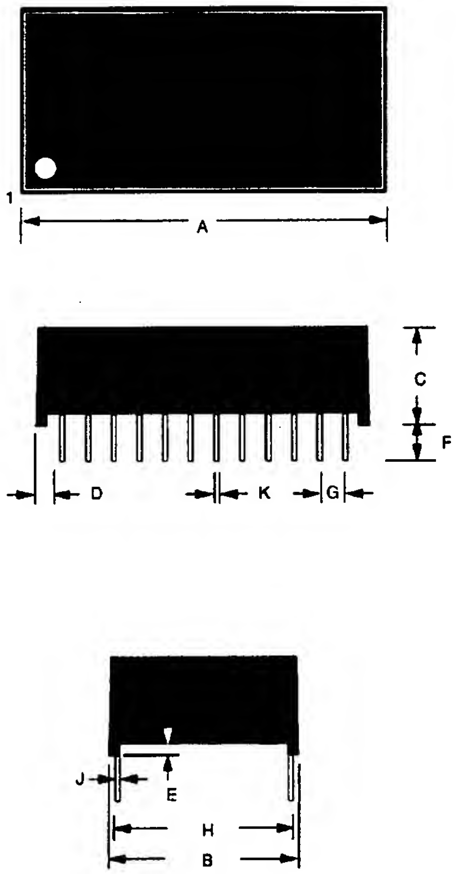
NOTES:

1) Voltages are referenced to ground.
2) Typical values are at 25°C and nominal supplies.
3) Outputs are open.
4) Data retention time is at 25°C.
5) Each DS1642 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
6) Real-time clock modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used to prevent damage to the crystal.

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

DS1642 24-PIN PACKAGE



PKG	24-PIN	
DIM.	MIN	MAX
A IN. MM	1.270 37.34	0.290 37.85
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.315 8.00	0.335 78.51
D IN. MM	0.075 1.91	0.105 2.67
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.140 3.56	0.180 4.57
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.010 0.25	0.018 0.45
K IN. MM	0.015 0.43	0.025 0.58

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600